regions and the second conductive type regions extend in a first direction, and wherein the first conductive type regions and the second conductive type regions are alternatively arranged in a second direction; forming a channel layer having a second conductive type on the super junction structure; forming a plurality of second trenches to penetrate the channel layer and to reach a corresponding first conductive type region, wherein the second trenches have a stripe pattern; forming a gate insulation film on an inner wall of each second trench, and forming a gate electrode on the gate insulation film in each second trench, so that the second trenches, the gate insulation film and the gate electrode provide a trench gate structure; implanting a first conductive type impurity into a surface portion of the channel layer; implanting a second conductive type impurity into another surface portion of the channel layer; and heating the substrate so that the second conductive type impurity in the channel layer is diffused, and a contact second conductive type region is formed in the another surface portion of the channel layer, which is opposite to a corresponding second conductive type region. The contact second conductive type region has an impurity concentration higher than the channel layer. In the heating of the substrate, the first conductive type impurity in the channel layer is diffused, and a first conductive type layer is formed in the surface portion of the channel layer. The first conductive type layer has the first conductive type, and contacts a sidewall of a corresponding trench. In the heating of the substrate, the second conductive type impurity in the second conductive type regions is diffused, and an embedded second conductive type region is formed in a corresponding second conductive type region. The embedded second conductive type region has an end, which protrudes into the channel layer and contacts the contact second conductive type region. The embedded second conductive type region has the other end, which is deeper than a bottom of a corresponding trench. The embedded second conductive type region has an impurity concentration higher than the channel layer, and has a maximum impurity concentration at a position in the corresponding second conductive type region.

[0153] In the above method, when the second conductive type region is embedded in the trench, the second conductive type region film is formed on the first conductive type region, and the second conductive type impurity is implanted in the second conductive type region film in the trench with using the second conductive type region film on the first conductive type region as a mask. Accordingly, it is not necessary to prepare a new mask, so that the manufacturing method is simplified.

[0154] While the invention has been described with reference to preferred embodiments thereof, it is to be understood that the invention is not limited to the preferred embodiments and constructions. The invention is intended to cover various modification and equivalent arrangements. In addition, while the various combinations and configurations, which are preferred, other combinations and configurations, including more, less or only a single element, are also within the spirit and scope of the invention.

What is claimed is:

1. A semiconductor device comprising:
- a substrate having a first conductive type;
- a plurality of first conductive type regions and a plurality of second conductive type regions disposed on the substrate, extending in a first direction, and alternately arranged in a second direction so that a super junction structure is provided;
- a channel layer having a second conductive type and disposed on the super junction structure;
- a first conductive type layer disposed in a first surface portion of the channel layer;
- a contact second conductive type region disposed in a second surface portion of the channel layer, which is opposite to a corresponding second conductive type region, and having an impurity concentration higher than the channel layer;
- a gate insulation film disposed on the channel layer;
- a gate electrode disposed on the gate insulation film;
- a surface electrode disposed on the channel layer;
- a backside electrode disposed on the substrate opposite to the super junction structure; and
- an embedded second conductive type region,
- wherein a current flows between the surface electrode and the backside electrode,
- wherein the embedded second conductive type region is disposed in a corresponding second conductive type region, protrudes into the channel layer, and contacts the contact second conductive type region, and
- wherein the embedded second conductive type region has an impurity concentration higher than the channel layer, and has a maximum impurity concentration at a position in the corresponding second conductive type region.

2. The semiconductor device according to claim **1**,
- wherein the embedded second conductive type region has an impurity concentration distribution.

3. The semiconductor device according to claim **1**,
- wherein the embedded second conductive type region has a cross section perpendicular to the first direction, and
- wherein an equivalent concentration line of the cross section has a predetermined curvature.

4. The semiconductor device according to claim **1**,
- wherein the embedded second conductive type region has a maximum width in the second direction, which is smaller than a maximum width of the corresponding second conductive type region in the second direction, and
- wherein the embedded second conductive type region is disposed in the channel layer and the corresponding second conductive type region.

5. The semiconductor device according to claim **4**,
- wherein the maximum width of the embedded second conductive type region in the second direction is smaller than a maximum width of the contact second conductive type region in the second direction.

6. The semiconductor device according to claim **1**,
- wherein the channel layer includes a plurality of channel forming layers, which are stacked,
- wherein the embedded second conductive type region includes a plurality of embedded second conductive type region forming layers, which are coupled with each other in a depth direction,
- wherein the depth direction is perpendicular to the first direction and the second direction, and
- wherein at least one of the embedded second conductive type region forming layers has a maximum impurity concentration at a position in the corresponding second conductive type region.

7. The semiconductor device according to claim **1**, further comprising:
- a cell portion; and
- an outer periphery portion,
- wherein the current flows between the surface electrode and the backside electrode in the cell portion,